

In Re Patent Application of:
D'ALBORE ET AL.
Serial No. 10/820,462
Filing Date: April 8, 2004

REMARKS

The Examiner is thanked for the careful examination of the present application and for recognizing that features of the invention distinguish it from the teachings of Wong et al. The Examiner helpfully pointed out that these features were not clearly recited in the claims. Accordingly, independent Claims 1, 16, and 25 have been amended to more clearly define the claimed invention over the prior art based upon the Examiner's helpful comments.

In view of the amendments made and the arguments presented in detail below, it is submitted that all claims are patentable.

I. The Amended Claims

Independent Claim 1, for example, is directed to a method for patching read only memory (ROM) instructions in an electronic system comprising a first non-volatile memory portion storing instruction groups defining patching functionalities, an extended memory portion storing extended instructions, and an additional memory portion.

The method comprises checking a flag stored in the additional memory portion. The flag indicates a need for executing the extended instructions in the extended memory portion. Processing of the ROM instructions in the first non-volatile memory portion and the extended instructions in the extended memory portion are alternated based upon the flag. Independent Claim 1 has been amended to recite the flag represents binary information associated to a subroutine that uses a patching mechanism residing at least initially in the

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first non-volatile memory and defined by the ROM instructions. Each patching mechanism has a respective flag associated therewith.

Independent method Claim 16 is similar to independent method Claim 1 and has been similarly amended. Independent device Claim 25 is similar to independent method Claim 1 and has been similarly amended.

II. The Claims Are Patentable

The Examiner rejected independent Claims 1, 16, and 25 over Wong et al. Wong et al. discloses a programmable memory that stores patches and vectors to determine a patch address. Wong et al. teaches mapping a portion of the patch code. Indeed, paragraph [0033] of Wong et al. provides:

"In this case, the patch code 420 located in the RAM 406 is outside the allowed operation instruction space of the UPC 402. In this case, the patch code 420 is mapped into unused ROM space." (Emphasis added).

In sharp contrast, independent Claims 1, 16, and 25 have been amended to recite a patching mechanism residing at least initially in the first non-volatile memory. The Wong et al. way includes patch code initially residing in volatile memory (RAM) which is, at a later point in time, mapped to ROM. Differently, the patching mechanism of independent Claims 1, 16 and 25 resides at least initially in the first non-volatile memory. Therefore, it cannot be argued that Wong et al. discloses the feature of a patching mechanism residing at least initially in the first non-volatile memory. Indeed, this

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distinction was helpfully noted by the Examiner in the present Office Action.

Accordingly, Wong et al. fails to disclose all features of independent Claims 1, 16, and 25, which are therefore patentable. Their respective dependent claims, which recite yet further distinguishing features, are likewise patentable and require no further discussion herein.

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III. CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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